Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A power switch having source, drain and gate terminals, the power switch comprising:

a first field-effect transistor (FET) having a first drain coupled to the drain terminal, a first source coupled to the source terminal, and a first gate;

a second FET having a second drain coupled to the drain terminal, a second source coupled to the source terminal, and a second gate, the second FET having a gate length (L_G) that is greater than or less than an L_G of the first FET and having a length of a drain (L_D) that is greater than or less than an L_D of the first FET; and

a control circuit coupled to the gate terminal, <u>and having a first control signal coupled to</u> the first gate[[,]] and <u>a second control signal coupled to</u> the second gate<u>, the first control signal and the second control signal being separate control signals, and the first control signal having a rising edge with a different timing than a rising edge of the second control signal</u>.

2. (Original) The power switch of claim 1, wherein the control circuit is configured to turn on the second FET before turning on the first FET.

3. (Original) The power switch of claim 1, wherein the control circuit is coupled to the drain terminal.

4. (Original) The power switch of claim 3, wherein the control circuit is configured to impose a fixed delay between turning on the first and second FETs.

5. (Original) The power switch of claim 4, wherein the control circuit is configured to delay turning on the first FET until the voltage between the drain and source terminals falls below a predetermined voltage.

6. (Original) The power switch of claim 1, wherein the control circuit is configured to turn off the second FET after turning off the first FET.

7. (Original) The power switch of claim 6, wherein the control circuit is configured to impose a fixed delay between turning off the first and second FETs.

8. (Original) The power switch of claim 1, wherein the first FET is designed for electrical performance superior to that of the second FET.

9. (Original) The power switch of claim 8, wherein the first FET is an n-type CMOS FET.

10. (Original) The power switch of claim 8, wherein the first FET is an LDMOS transistor.

11. (Original) The power switch of claim 1, wherein the second FET is designed for reliability performance superior to that of the first FET.

12. (Original) The power switch of claim 1, wherein the first and second FETs are implemented as a single monolithic device.

13. (Original) The power switch of claim 1, wherein the first and second FETs and the control circuit are implemented as a single monolithic device.

14. (Original) The power switch of claim 1, wherein the second FET has an L_G greater than an L_G of the first FET and an L_D greater than an L_D of the first FET.

15. (Original) The power switch of claim 1, further comprising:

a current sensing circuit configured to disable the first FET when the load current at the drain terminal is below a predetermined threshold current.

16. (Original) The power switch of claim 15, wherein the current sensing circuit is configured to switch the second FET when the first FET is disabled.

17. (Original) The power switch of claim 1, wherein the first FET has an area less than the area of the second FET.

18. (Original) The power switch of claim 1, wherein the second FET has an L_G smaller than an L_G of the first FET and an L_D smaller than an L_D of the first FET.

19. (Original) The power switch of claim 1, wherein L_D is a measurement that represents spacing between an N+ drain implant and a gate of a given FET.

20. (Original) The power switch of claim 1, wherein the second FET is more resilient to hot-carrier degradation than the first FET.

21. (Original) The power switch of claim 1, wherein the second FET has a wider safe operating area (SOA) than the first FET.

22. (Original) The power switch of claim 1, wherein the second FET has a higher avalanche energy rating than the first FET.

23. (Currently Amended) A method of operating a power switch having a source terminal and a drain terminal, comprising:

turning on a first field-effect transistor (FET) using a first control signal having a first rising edge, the first FET having [[that has]] a first drain coupled to the drain terminal, a first source coupled to the source terminal, and a first gate;

turning on a second FET using a second control signal having a second rising edge while the first FET is on, the second control signal being separate from the first control signal, the second rising edge having a different timing than first rising edge, the second FET having a second drain coupled to the drain terminal, a second source coupled to the source terminal, and a second gate, the second FET having a gate length (L_G) that is greater than or less than an L_G of the first FET and having a length of a drain (L_D) that is greater than or less than an L_D of the first FET;

turning off the second FET using the second control signal while the first FET is on; and

turning off the first FET using the first control signal.

24. (Original) The method of claim 23, wherein the turning on and off the second FET and first FET includes directing signals from a control circuit to the first and second gates.

25. (Original) The method of claim 24, further comprising receiving a signal in the control circuit from the drain terminal.

26. (Original) The method of claim 23, further comprising delaying turning on the second FET for a predetermined period of time after turning on the first FET.

27. (Original) The method of claim 23, further comprising determining a voltage between the drain and source terminals.

28. (Original) The method of claim 27, further comprising delaying turning on the second FET until the voltage between the drain and source terminals falls below a predetermined voltage.

29. (Original) The method of claim 23, further comprising delaying turning off the first FET for a predetermined period of time after turning off the second FET.

30. (Original) The method of claim 23, further comprising determining a load current at the drain terminal.

31. (Original) The method of claim 30, further comprising disabling the second FET when the load current at the drain terminal is below a predetermined threshold current.

32. (Original) The method of claim 31, further comprising switching the first FET when the second FET is disabled.

33. (Original) The method of claim 23, wherein the second FET is designed for electrical performance superior to that of the first FET.

34. (Original) The method of claim 23, wherein the helper FET is designed for reliability performance superior to that of the main FET.

35. (Original) The method of claim 23, wherein the first FET and the second FET are implemented as a single monolithic device.

36. (Original) The method of claim 23, wherein the first FET has an area less than the area of the second FET.

37. (Original) The method of claim 23, wherein L_D is a measurement that represents spacing between an N+ drain implant and a gate of a given FET.

38. (Original) The method of claim 23, wherein the second FET is an n-type CMOS FET.

39. (Original) The method of claim 23, wherein the second FET is an LDMOS transistor.

40. (New) The power switch of claim 1, wherein the control circuit includes one or more buffer stages for delaying the timing of the rising edge of the first control signal relative to the timing of the rising edge of the second control signal.

41. (New) The method of claim 23, further comprising using one or more buffer stages to delay the timing of the rising edge of the second control signal relative to the timing of the rising edge of the first control signal.